Amendments to the Specification:

Please replace paragraph [0033] with the following amended paragraph:

[0033] The Figure 5A system may include several processors, of which only two, processors 40, 60 are shown for clarity. Processors 40, 60 may include level one caches 42, 62, and fork predictors 500 and 501. Fork predictors 500 and 501 are configured similarly to the fork predictors described above with respect to fork predictors 150 and 230, and are configured to perform embodiments of the method described herein. The Figure 5A system may have several functions connected via bus interfaces 44, 64, 12, 8 with a system bus 6. In one embodiment, system bus 6 may be the front side bus (FSB) utilized with Pentiurn@ class microprocessors manufactured by Intel@ Corporation. In other embodiments, other buses may be used. In some embodiments memory controller 34 and bus bridge 32 may collectively be referred to as a chipset. In some embodiments, functions of a chipset may be divided among physical chips differently than as shown in the Figure 5A embodiment.

Please replace paragraph [0035] with the following amended paragraph:

[0035] The Figure 5B system may also include several processors, of which only two, processors 70, 80 are shown for clarity. Processors 70, 80 may each include a local memory channel hub (MCH) 72, 82 to connect with memory 2, 4. Processors 70, 80 include fork predictors 500 and 501. Fork predictors 500 and 501 are configured similarly to the fork predictors described above with respect to fork predictors 150 and 230, and are configured to perform embodiments of the method described herein. Processors 70, 80 may exchange data via a point-to-point interface 50 using point-to-point interface circuits 78, 88. Processors 70, 80 may each exchange data with a chipset 90 via individual point-to-point interfaces 52, 54 using point to point interface circuits 76, 94, 86, 98. Chipset 90 may also exchange data with a high performance graphics circuit 38 via a high-performance graphics interface 92.